Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.010”**

**.010”**

**ANODE**

**.003 X .003”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .003” X .003”**

**Backside Potential: CATHODE**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .010” X .010” DATE: 11/10/21**

**MFG: VISHAY THICKNESS .006” P/N: 1N5712**

**DG 10.1.2**

#### Rev B, 7/1